AMENDMENT TO THE CLAIMS

This listing of claims replaces all prior versions and listing of claims in the application:

1. An apparatus for testing a device under test (DUT) having a plurality of pins, the apparatus comprising:

a clock having a clock cycle

a plurality of pin electronics channels (PEs) capable of coupling to the plurality of pins on the DUT;

a plurality of timing and format circuits (T/Fs) each capable of mapping a signal to one of the plurality of PEs;

a pattern memory capable of storing a number of bits for testing the DUT, the pattern memory having a plurality of outputs capable of outputting the bits to test the DUT; and

a pattern scrambler coupled between the plurality of outputs and the plurality of T/Fs, the pattern scrambler capable of being programmed to couple bits from any one or more of the plurality of outputs to any one or more of the plurality of T/Fs, to provide a test pattern to the DUT having a programmable width of from 1 bit wide to a width equal to the number of the plurality of PEs.

2. An apparatus according to Claim 1, wherein the pattern memory has *n* outputs and a capacity of *m* x *n* bits, and wherein the pattern scrambler is capable of being programmed to provide test patterns having a depth of from *n* x *m* bits with a width of 1 bit to a depth of *m* bits with a width of *n* bits.

3. An apparatus according to Claim 2, wherein the pattern scrambler is capable of changing at least one of the width or the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

4. An apparatus according to Claim 1, wherein the pattern scrambler is capable of coupling bits from any one of the plurality of outputs to any one of the plurality of PEs, and wherein the pattern scrambler is capable of changing bits coupled to one or more of the plurality of PEs on a cycle-by-cycle basis for each clock cycle of the test system.

5. An apparatus according to Claim 1, wherein the pattern memory is capable of being operated to simultaneously provide a logic vector memory (LVM) for storing logic vectors of a number of bits and having a width and a depth, and a scan memory for storing scan vectors of a number of bits and having a width and a depth.

6. An apparatus according to Claim 5, wherein logic vectors stored in the LVM and the scan vectors stored in the scan memory comprise different widths.

7. A pattern generator for testing at least one device under test (DUT) having a plurality of pins, the pattern generator comprising:

a pattern memory capable of storing a number of bits for testing the DUT, the pattern memory having a plurality of outputs capable of outputting the bits to test the DUT; and

a pattern scrambler coupled between the plurality of outputs and the plurality of pins on the DUT, the pattern scrambler capable of being programmed to couple bits from any one or more of the plurality of outputs to any one or more of the plurality of pins on the DUT, to provide a test pattern to the DUT having a programmable width of from 1 bit wide to a width equal to the number of the plurality of outputs.

8. A pattern generator according to Claim 7, wherein the pattern memory has *n* outputs and a capacity of *m* x *n* bits, and wherein the pattern scrambler is capable of being programmed to provide test patterns having a depth of from *n* x *m* bits with a width of 1 bit to a depth of *m* bits with a width of *n* bits.

9. A test system comprising a pattern generator according to Claim 8, the test system further comprising a clock having a clock cycle, and wherein the pattern scrambler is capable of changing at least one of the width or the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

10. A pattern generator according to Claim 7, wherein the pattern scrambler is capable of being programmed to couple bits from each one of the plurality of outputs to one or more of the plurality of pins on one or more DUTs.

11. A test system comprising a pattern generator according to Claim 10, the test

system further comprising a clock having a clock cycle, and wherein the pattern scrambler is capable of changing bits coupled to one or more of the plurality of pins on one or more DUTs on a cycle-by-cycle basis for each clock cycle of the test system.

12. A pattern generator according to Claim 7, wherein the pattern scrambler is capable of being operated to simultaneously provide a logic vector memory (LVM) for delivering logic vectors of a number of bits and having a width and a depth, and a scan memory for delivering scan vectors of a number of bits and having a width and a depth.

13. A pattern generator according to Claim 12, wherein logic vectors delivered from the LVM and the scan vectors delivered from the scan memory comprise different widths.

14. A test system comprising a pattern generator according to Claim 12, the test system further comprising a clock having a clock cycle, and wherein the width of the logic vectors delivered from the LVM and the scan vectors delivered from the scan memory can be changed by the pattern scrambler on a cycle-by-cycle basis for each clock cycle of the test system.

15. A pattern generator according to Claim 7, wherein the pattern scrambler is capable of being programmed to couple a data bit of one of the plurality of outputs, output *n,* to one or more of the plurality of pins on the DUT, while strobe and I/O control bits of output *n* are coupled to one or more of the plurality of pins on the DUT, different from the one or more of the plurality of pins on the DUT to which the data bit is coupled, and wherein the I/O control bit is capable of being used as an expect data bit on the one or more of the plurality of pins on the DUT to which it is coupled.

16. A test system comprising a pattern generator according to Claim 7, the test system further comprising a clock having a clock cycle, and wherein the pattern scrambler is capable of switching bits from any one of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle,

whereby test patterns are provided to the DUT at a rate at least twice that of the clock cycles.

17. A method for testing a device under test (DUT) using a test system including a pattern memory having a plurality of outputs equal to *n*, and a pattern scrambler coupled between the plurality of outputs and a plurality of pins on the DUT, the method comprising steps of:

storing a number of bits for testing the DUT in the pattern memory; and

programming the pattern scrambler to ~~output bits from~~ select, for each pin of the DUT, one or more bits from all of the plurality of outputs to be coupled to one or more of the plurality of pins on the DUT, and to provide a test pattern to the DUT having a programmable width of from 1 to *n* bits.

18. A method according to Claim 17, wherein the pattern memory has a capacity of *m* x *n* bits, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to provide test patterns having a depth of from *n* x *m* bits with a width of 1 bit to a depth of *m* bits with a width of *n* bits.

19. A method according to Claim 18, wherein the test system further comprises a clock having a clock cycle, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to change at least one of the width or the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

20. A method according to Claim 17, wherein the test system further comprises a clock having a clock cycle, and wherein the pattern scrambler is capable of coupling bits from any one of the plurality of outputs to any one of the plurality of pins on the DUT, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to change bits coupled to one or more of the plurality of pins on the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

21. A method according to Claim 17, wherein the pattern memory is capable of being operated to simultaneously provide a logic vector memory (LVM) and a scan memory, and wherein the step of storing a number of bits for testing the DUT in the pattern memory comprises the step of storing in the LVM logic vectors of a number of bits and having a width and a depth, and storing in the scan memory scan vectors of a number of bits and having a width and a depth.

22. A method according to Claim 21, wherein the step of storing a number of bits for testing the DUT in the pattern memory comprises the step of storing LVM vectors and the scan vectors having different widths.

23. A method according to Claim 11, wherein the test system further comprises a clock having a clock cycle, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to switch bits from any one of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle,

whereby test patterns are provided to the DUT at a rate at least twice that of the clock cycles.